

財團法人國防工業發展基金會 便簽

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- 一、國立中山大學光電工程學系林建佑博士生畢業論文公告案。
- 二、中山大學光電工程學系林建佑博士原支領本會 108 年度國防工業獎學金，渠於今(110)年 8 月 24 日畢業離校(如附呈 1)，畢業後前往「台灣積體電路製造股份有限公司(台積電)」服研發替代役。台積電市值全球十大，半導體晶圓代工全球排名第一，為國際知名晶圓代工半導體製造廠。
- 三、林博士畢業論文題目「前瞻式金氧半電容器與鰭式場電晶體之電性分析與可靠度機制研究」(英文版)，按本會「國防工業獎學金發放作業規定」第五點獎學金受領人義務(三)規定，提供畢業論文 2 本及電子檔，並於論文致謝誌中表達對本會之感謝。另按同規定第七點成果運用，畢業論文無償提供本會或本會指定之公法人、政府機關(構)運用。(如附呈 2)
- 四、林博士畢業論文主頁及中、英文摘要、目錄等擬於本會網站公告(如附件)，提供國防部研究單位(如：國防部軍備局、中科院、國防安全研究院、軍事院校等)有需求可洽本會索取。
- 五、請核示。

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國立中山大學光電工程學系

博士論文

Department of Photonics

National Sun Yat-Sen University

Doctorate Dissertation

前瞻式金氧半電容器與鰭式場效電晶體之

電性分析與可靠度機制研究

Investigation on Electrical Analysis and Reliability Mechanisms
of Advanced MOSCAP and FinFETs

研究生：林建佑

Chien-Yu Lin

指導老師：張鼎張 博士

Dr. Ting-Chang Chang

中華民國 110 年 8 月

August 2021

論文審定書

國立中山大學研究生學位論文審定書

本校光電工程學系博士班

研究生林建佑（學號：D043090002）所提論文

前瞻式金氧半電容器與鰭式場效電晶體之電性分析與可靠性機制研究
Investigation on Electrical Analysis and Reliability Mechanisms of
Advanced MOSCAP and FinFETs

於中華民國 110 年 8 月 21 日經本委員會審查並舉行口試，符合博士學位論文標準。

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致謝

轉眼間 6 年，碩博生涯也即將邁入尾聲，這幾年在半導體以及人生經歷也內化成現在的我，終於要以嶄新的自己邁開步伐接受社會的挑戰啦。從小時候懵懂無知念著理工科電機，只知道需要個碩士學位以符合工作需求，尋找實驗室時在張鼎張老師的介紹下，好像發現一個新世界，能支撐我所憧憬夢想的未來，有興趣且有動力能投入其中研究的產業環境，還能夠把研發的內容化做生活處處可見的 IC 晶圓各種科技產物，想起來就很有成就感，因此在大學畢業的年紀就決定未來 5 年所要投資自己的道路，有目標的訂立執行起來也不會迷惘；童年在海邊長大的我，海洋對我來說永遠都看不膩，替我充電且吸引著我，從實驗室看出的西子灣景色著實令人著迷，中山大學博士班的生涯就此展開。

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林建佑 謹識

前瞻式金氧半電容器與鰭式場效電晶體之 電性分析與可靠度機制研究

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摘要

自 1960 年，世界上第一顆電晶體由 Bell 實驗室的 D. Kahng 和 Martin Atalla 首次實作成功。此時電晶體的通道長度還維持在 25 微米 (μm)，氧化層厚度為 100 奈米(nm)，五年後，Intel 創辦人之一 Gordon Moore 提出 “Moore’s Law”，其內容為：積體電路上可容納的電晶體，約每隔兩年便會增加一倍，7 奈米的鰭式電晶體(FinFET)已經順利量產並應用至高端電子產品當中。可隨著世代演進，微縮已至物理極限也不能迎合的更高操作速度的需求，所以將從材料本質上追求載子移動率更高的材料或者進行元件結構的設計，來提升元件性能。

第三章我們研究了矽通道和矽鍺 (SiGe) 通道 MOSCAP 之間的電容 - 電壓 (C-V) 特性，顯著的平帶電壓 (V_{FB}) 偏移和 C-V 高台(hump)僅出現在 SiGe 通道器件中，我們發現這兩種元件之間的 V_{FB} 偏移取決於半導體基板與金屬公函數的差異，我們提出了一個缺陷分佈模型來解釋異常現象，通過改變 C-V 測量頻率並使用電導法萃取能帶內的缺陷態密度分佈來證明所提出的模型，我們還對 C-V 中的這種異常高台特性提出了額外的解釋，Silvaco-TCAD 元件模擬軟體的

結果也進一步證實我們的模型假設。

為了進一步提高元件性能，於第四章我們開發了用於 Si 和 SiGe-MOSCAP 元件的低溫高壓（LTHP）氫化的缺陷鈍化技術。LTHP 處理法是處於液態和氣態間的特殊材料狀態，其結合了液體的高溶解度優點以及氣體的高穿透能力，將欲修補元素帶入元件並增強元件品質及性能。我們認為 LTHP 氫化處理可以修復 SiO_2/SiGe 界面間的斷鍵。利用電導法萃取初始狀態和處理後的缺陷密度，可以觀察到缺陷密度顯著降低。並提出能帶模型，且模擬結果也驗證了深能級缺陷的修復。我們還調變了不同的處理條件，包括溫度，時間和氫濃度，並在 Si 和 SiGe 通道 MOSCAP 中找到最佳的缺陷鈍化參數。

相較於改變元件材料，第五章節我們對 FinFETs 結構元件進行了些研究。本部分研究了經熱載子應力（HCS）後，N 型鰭式場效電晶體（FinFETs）有異常基極電流（ I_{sub} ）上升的現象。傳統上在 HCS 之後，飽和區的汲極電流和 I_{sub} 會持續減小。然而在這項研究中，出現了 I_{sub} 首先減少，然後逐漸上升的異常現象。我們將透過不同的測量方法研究此異常行為，並且發現是由於陷阱輔助穿隧的機制。本研究首先使用不同的工作電壓來證明所提出的模型，然後利用變溫度應力條件來驗證。最後利用介面電流測量找出缺陷產生的位置。

第六章節中，隨著器件不斷縮小到接近 20 nm 的通道長度。研究了基極電流與短溝道鰭式場效應晶體管（FinFET）退化的關係。從 $\log I_D\text{-}V_G$ 圖中，藉由熱載子劣化前後的閾值電壓偏移量辨別出氧化物陷阱（Not）和界面態陷阱（Nit）的變化。在不同器件尺寸的不同應力條件下，可以分別觀察到 Not 和 Nit 的變化趨勢。發現短溝道 FinFET 結構器件的 HCS 退化機制以 MVE 為主。隨著應力 V_G 增加，閾值電壓變化更嚴重。而缺陷在通道中產生得更均勻。

關鍵字：金氧半場效電晶體、矽鍺通道、超臨界處理、缺陷萃取、鰭式電晶體、熱載子劣化、偏壓不穩定性。

Investigation on Electrical Analysis and Reliability

Mechanisms of Advanced MOSCAP and FinFETs

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Abstract

Since 1960, the first metal-oxide-semiconductor-field-effect transistors (MOSFETs) in the world were invented by Kahng and Atalla in Bell Lab. The length of transistor is 25 μm , and thickness of gate oxide is 100nm. Nowadays, MOSFETs with low power consumption, low cost and easy to scale down, they have become the main component of ultra-large-scale integration (ULSI) circuits. In 1965, Gordon Moore, one of Intel's founders, first proposed Moore's Law: The number of devices per integrated circuit will doubling every year. The 7 nm fin transistor (FinFET) has been mass-produced and applied to advance electronic products. With the evolution of the IC technology, the miniaturization has reached the demand of higher operating speeds that cannot cater the physical limit. As a result, the material of intrinsic performance with higher carrier mobility would be attempted or the design of the device structure would be conducted in order to improve devices' performance.

Therefore, in the first part, we studied the capacitance - voltage (C-V) characteristics between silicon channel and silicon-germanium (SiGe) channel MOSCAPs. In comparison of both devices, significant flatband voltage (V_{FB}) shifts and a C-V plateau were observed only in the SiGe-channel device. We found that the V_{FB} shift between these two devices is determined by the difference in substrate work-function values against metal. We propose a defect distribution model to explain abnormal phenomenon. The proposed model was proved by changing the frequency of C-V measurement and extracting the interface state density distributions within the energy band using the conductance method. We also provide additional explanation of this anomalous plateau in the C-V measurements. Moreover, the result of Silvaco-TCAD device simulation tool also supports our model. The hypothesis is further confirmed by the defect position and defect quantity in the energy band.

To further improve the device performance, we developed a Low-Temp-High-Pressure (LTHP) of hydridation treatment used for Si- and SiGe- MOSCAP devices in the second part. The LTHP treatment (LTHPT) is an unique material state that uses the coexistence characteristics of liquid and gaseous states. It combines the advantages of the high permeability capability and also high liquid solubility of gas to enhances the device performance. We think that the LTHPT of hydridation can effectively passivate dangling bonds in the SiO_2/SiGe interface. Utilizing the conductance method to extract D_{it} between pristine devices and the devices after treatment, a significant reduction in D_{it} can be observed. Subsequently, the energy diagram model is proposed, and the simulation result verifies that the deep state defects are mended. We also adjust different treatment condition including temperature, time and hydrogen concentration, and find the optimal parameters in Si- and SiGe-channel MOSCAP.

Instead of changing the device material, we also did some research on optimizing

structure of fin field effect transistors (FinFET). This part studies the mechanism of uncommon body current (I_B) after hot carrier stress (HCS) in FinFETs. Generally, I_B will continually decrease with the drain current after HCS. However, in this work, I_B first declines then showed a gradual unusual ascent. This unusual I_B behavior was studied through different measurement methods, and it was speculated that is was caused by trap-assisted tunneling. First, utilizes different operating bias to confirm the model we proposed, then applies different temperature during stress which further verify the model. Finally, junction current can also be measured to determine the location of the defect generation.

In the final section, as device's channel length continually shrinks to around 20 nm. The relationship between body current and degradation of short channel fin field transistor (FinFET) was widely studied. From $\log I_D$ - V_G diagrams, the change of oxide trap (N_{ot}) and interface state trap (N_{it}) are calculated from threshold voltage shift before and after stress. Under different stress conditions of different device dimensions, the trends of N_{ot} and N_{it} will be able to be observed, respectively. However, as stress V_G increases, the threshold voltage shifts more severely. From these results, it is found that the HCS degrade mechanism of short channel FinFET structure device is dominate by MVE. As stress V_G increases, the threshold voltage shifts more severely. Moreover, defect generates more uniform in the channel.

Keywords: MOSFETs 、 SiGe-channel 、 LTHPT 、 D_{it} extraction 、 FinFETs 、 Hot Carrier Instability 、 BTI.

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