



## 國立中山大學物理學系

### 博士論文

Department of Physics

National Sun Yat-sen University

Doctorate Dissertation

次世代電阻式記憶體與  
氮化鎵高電子遷移率電晶體物理機制研究

Research on Physical Mechanism of

Next Generation Resistive Random Access Memory and GaN High  
Electron Mobility Transistor

研究生：鄭皓軒

Hao-Xuan Zheng

指導教授：張鼎張 博士

Dr. Ting-Chang Chang

中華民國 111 年 01 月

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# 論文審定書

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Memory and GaN High Electron Mobility Transistor

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## 摘要

近年來 5G 通訊、人工智慧物聯網(AIoT)以及車用電子各項技術蓬勃發展，在高速運算、儲存容量與大功率操作的需求下，記憶體元件與功率電晶體的發展相當重要。在記憶體方面，隨著人工智慧物聯網時代的來臨，微控制器(MCU)將扮演相當重要的角色，而微控制器需使用大量的嵌入式記憶體(Embedded Memory)，嵌入式記憶體需要低操作功耗、高操作速度，並且能與半導體製程整合，在次世代記憶體中，電阻式記憶體最具有潛力。而在功率電晶體方面，過去以矽基元件的設計和技術開發經過了多次結構和製程優化更新，已逐漸接近矽材料的極限。而氮化鎗(GaN)為寬能隙(Wide Band-gap)半導體材料的代表之一，相較於矽材料，具有寬能隙(bandgap)、高臨界電場(critical electric field)、高電子飽和速度(electron saturation velocity)等特性，在電動車與 5G 通訊方面為極具優勢的材料，以氮化鎗(GaN)為基底的高電子遷移率電晶體(High Electron Mobility Transistor, HEMT)日漸受到重視，顯現出氮化鎗在商業市場上的重要性以及未來的發展性。本論文針對電阻式記憶體以及氮化鎗高電子遷移率電晶體之性能進行相關研究。

RRAM 的元件目前以電晶體控制其開關(1T1R)作為嵌入式記憶體的主要結構。隨著莫爾定律的發展，電晶體的通道不斷的微縮，電晶體可承受的電壓會越來越小，可能會逼近 RRAM 最大的操作電壓 - 形成電壓(Forming Voltage)，因此，如何降低形成電壓就會是一個重要的問題。本論文提出利用交流訊號進行 Forming 的步驟，使 RRAM 的 Forming 電壓下降，並且更進一步的設計出理想的操作波形，應

用於嵌入式電阻式記憶體中。另一方面，由於嵌入式電阻式記憶體是 RRAM 串聯一電晶體，在 Reset 過程中，RRAM 所獲得的電壓增加，造成電晶體的 VGS 減少，電晶體進入飽和區，使 RRAM 無法有效地增加操作窗口。因此，RRAM 的操作窗口會受到電晶體的限制。除此之外，電晶體不只影響 RRAM 的操作窗口，也會影響 RRAM 的阻態分部，因此，了解嵌入式電阻式記憶體操作過程中，RRAM 與電晶體之間的關係，能夠有效降低嵌入式電阻式記憶體操作過程中電晶體的跨壓，就可以設計出低功耗/高性能嵌入式電阻式記憶體的架構。

在氮化鎵高電子遷移率電晶體方面，考量安全因素元件的起始電壓須大於 0，因此 p-GaN HEMT 因可達增強型(Enhancement-Mode, E-mode)為主要發展的元件，但是元件在關態時會產生嚴重的漏電流，故如何抑制元件漏電流是一重要議題。研究中發現 p-GaN HEMT 元件具有駝峰效應。分析其原因係在元件保護層中，因製程所產生的氫擴散至 p-GaN 層，進而產生次通道(Sub-channel)效應造成較大關態漏電。另一方面，p-GaN HEMT 閘極常見有 Ni、Au 和 TiN 等材料，不同材料間基本物理特性會影響元件的基本性能。然而，閘極金屬製程可能因為前驅物或電漿的轟擊，導致元件有前驅物殘留的污染、不平整的表面和較差的介面品質。此章節主要討論 p-GaN HEMT 漏電成因與不同閘極金屬製程對於之性能的影響。

關鍵字：電阻式記憶體、嵌入式記憶體、功率半導體元件、氮化鎵高電子遷移率電晶體、氫效應

# **Abstract**

In recent years, 5G communications, artificial intelligence Internet of Things (AIoT) and electric vehicle technologies have flourished, and the demand for high-speed computing, storage capacity, and high-power operation has increased. The development of memory devices and power transistors is paramount. In terms of memory, with the advance of AIoT, micro control units (MCUs) will play a very important role, and MCU needs to incorporate a lot of embedded memory. Embedded memory requires low power consumption, high operating speed, and it can be integrated with semiconductor manufacturing processes. Among the next-generation memory, resistive random access memory (RRAM) has been one of the most potential candidates. In terms of power transistors, the development of silicon-based devices has undergone many structural and process optimization, and they have gradually approached the limit of silicon-based devices. Gallium nitride (GaN) is one of the representatives of wide band-gap semiconductor materials. Compared with silicon materials, it has a wide bandgap, high critical electric field, and high electron saturation velocity. It is a highly advantageous material for electric vehicles and 5G communications. High Electron Mobility Transistor (HEMT) based on GaN is gaining more and more attention, showing the importance of GaN in the commercial market and its future development. This work conducts related research on the performance of RRAM and GaN HEMT.

RRAM currently uses a transistor to control its switch (1T1R) as the main structure of the embedded memory. With the development of Moore's law, the channel length of transistors is constantly shrinking, and breakdown (operating) voltage of the transistors will become smaller. It may approach the maximum operating voltage of RRAM-forming voltage. Therefore, how to reduce the forming voltage is an important issue. This study proposes the steps of using AC signals for forming process to reduce the forming voltage. Then, I further design the ideal operating waveform and apply it to the RRAM array. On the other hand, during the reset process, the voltage obtained by the RRAM has increased, causing the  $V_{GS}$  of the transistor to decrease, and the transistor is thereby turned off, making the RRAM unable to effectively increase the operating window. Therefore, the operating window of the RRAM is limited by the transistor. In addition, the transistor not only affects the operating window of the RRAM but also affects the resistance state of the RRAM. Therefore, understanding the relationship between RRAM and transistor during the operation of 1T1R can effectively reduce the cross voltage of the transistor. It can facilitate the design of a low-power/high-performance embedded memory architecture.

In terms of GaN HEMT, considering safety factors, the threshold voltage of the power device must be greater than 0. The p-GaN HEMT has more the most investigation due to enhancement-mode (E-mode) properties. However, a serious leakage current is

generated when the device is in the off state, so how to suppress the leakage current of the device is an important issue. In this study, p-GaN HEMT devices have also presented a hump effect. The orientation of the hump is that the hydrogen diffuses into the p-GaN layer during the ILD process, which generates a sub-channel effect and causes a large off-state leakage. On the other hand, p-GaN HEMT gates metal often is selected as Ni, Au, and TiN. The physical properties of different materials will affect the performance of the device. However, the gate metal process may be bombarded by precursors or plasma, resulting in residual contamination of the precursors, uneven surfaces, and poor interface quality. This chapter mainly discusses the causes of p-GaN HEMT leakage and the impact of different gate metal processes on its performance.

Keywords: Resistive Random Access Memory (RRAM), Embedded Memory, Power device, Gallium nitride high electron mobility transistors (GaN HEMT), Hydrogen effect

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