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異質接面通道非晶態銦鎵鋅氧薄膜電晶體於顯示器和記憶體應用之元件開發

Amorphous InGaZnO Thin-Film Transistors for Display and Memory Applications via Heterojunction Channels

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於中華民國 113 年 1 月 23 日經本委員會審查並舉行口試，符合博士學位論文標準。

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摘要

非晶態銦鎵鋅氧薄膜電晶體因其具有高載子傳輸率、極低關態漏電、大面積高均勻性、與可見光高透明度等材料特性，使其成為顯示器內像素開關與有機發光二極體之電流驅動等元件的重要角色。不僅如此，除了顯示器元件外，銦鎵鋅氧化物半導體因其具有低製程溫度的優勢，更是在邏輯晶片的後段製程中扮演著不可或缺的重要元件。然而，儘管銦鎵鋅氧化物半導體具有出色的元件特性，長時間操作下的不穩定性仍然是一項嚴峻的挑戰。截至目前為止，已經有許多文獻透過分析直流偏壓等靜態操作，釐清銦鎵鋅氧化物半導體在長時間操作下的元件劣化行為，並歸納在電應力、照光、自熱效應、與環境氣氛等狀況下的劣化物理模型。但隨著新一代擴增實境/虛擬實境等顯示技術以及邏輯晶片等技術的發展，銦鎵鋅氧化物半導體在高頻率/高切換速率下的元件性能和可靠性變得格外重要，使得先前研究於各式靜態操作下所提出之相關物理模型需加以改善與修正。因此，本論文將分析在高頻率/高切換速率下銦鎵鋅氧化物半導體元件的劣化現象，並提出相對應的物理模型。此外，我們將探討銦鎵鋅氧化物半導體元件於提升操作速率而改變結構時所面臨的各式製程或元件可靠度問題，並致力於開發高性能和高穩定性的非晶態銦鎵鋅氧半導體元件，使其能夠適用於各種應用場景。

於本論文的第一部分中，我們將探討蝕刻終止層結構之非晶態銦鎵鋅氧薄膜電晶體在動態切換下的元件劣化行為。在交流偏壓操作下，我們發現元件具有嚴重的閾值電壓漂移，而直流偏壓操作下，元件具有高穩定性。為了進一步釐清其元件劣化模型，本論文針對不同操作波型、元件結構相依性、與操作溫度進行了系統性的討論。結果表明，當元件從聚積態到空乏態的轉換過程中，電子將被蝕刻終止層之介面缺陷所捕獲。這一行為源自於短切換時間下，通道層沒有足夠的時間形成空乏層。因此，在切換到關態電壓後，於元件裡的剩餘電荷將於關態時的大閘極偏壓下進行捕獲行為。

於本論文第二部分中，我們將探討具銅電極之非晶態銦鎵鋅氧薄膜電晶體的

正偏壓應力不穩定性。為了提升顯示器之操作頻率，一般將選擇導電率更高之銅金屬取代鋁金屬，達到降低金屬導線之電阻-電容延遲之效益。然而，我們發現全銅電極之非晶態銦鎵鋅氧薄膜電晶體，在正偏壓操作下會使銅金屬閘極內部之銅離子擴散至閘極絕緣層中。我們透過對正偏壓應力過程中之各階段閘極漏電進行電流擬合，以分析此元件劣化行為。此外，為了更進一步觀測絕緣層中銅離子的擴散行為，我們亦透過聚焦離子束獲得元件橫截面，並以穿透式電子顯微鏡進行材料分析，透過其材料分析，觀測銅離子於氧化層之擴散行為。

於本論文第三部分中，我們透過應用異質接面之通道層實現了高性能與高可靠度的上閘極結構非晶態銦鎵鋅氧薄膜電晶體。我們所提出之異質接面通道為透過兩層不同金屬比例的銦鎵鋅氧薄膜堆疊而成。由結果表明，當引入富鋅-銦鎵鋅氧薄膜於元件通道前側時，此層可以做為氫原子擴散阻隔層，不僅能有效抑制短通道下的氫擴散行為，並有效抑制氧化層中的垂直電場。為進一步驗證此現象，本論文透過 Silvaco TCAD 元件模擬，系統性地討論異質接面通道薄膜電晶體之元件特性與可靠度。

於本論文第四部份中，我們藉由具異質接面通道層之非晶態銦鎵鋅氧薄膜電晶體，實現一高性能非揮發式光電記憶體元件。我們透過異質接面之載子侷限特性，成功將通道載子與電荷儲存層分離至元件前側與背側中。該記憶體元件具有 4.6 V 的記憶窗口、10^6 的讀取窗口、與小於 20V 的操作電壓需求。在儲存電荷能力方面，此記憶體具有大於 10 年的記憶時間與超過 1000 次的反覆操作能力。

關鍵字：薄膜電晶體、交流操作、銅擴散、異質接面、非揮發性記憶體、銦鎵鋅氧

Abstract

Amorphous indium-gallium-zinc oxide thin-film transistors are crucial components in display products owing to their exceptional material properties, including high carrier mobility, extremely low off-state leakage current, large-area uniformity, and high transparency to visible light. Therefore, they play essential roles in pixel switches of displays and driving current sources of organic light emitting diodes. Furthermore, owing to its advantage of low fabrication temperature, indium-gallium-zinc oxide semiconductors have become indispensable devices in the back-end-of-line of logic chips. However, despite the outstanding performances of indium-gallium-zinc oxide semiconductors, their long-term stability remains a challenging issue. To date, numerous studies have elucidated the deterioration of indium-gallium-zinc oxide semiconductors after long-term operation. These studies include analysis of stress conditions under direct current bias stresses, light irradiation, self-heating effects, or environmental atmospheres. Nevertheless, with the evolution of new-generation technologies such as augmented reality/virtual reality displays and its applications in advanced logic chips, their reliability under high-frequency/high-switching-rate conditions have become particularly significant. Therefore, this dissertation will focus on analyzing the deterioration of indium-gallium-zinc oxide semiconductor devices under these conditions and propose corresponding physical models. Additionally, within this dissertation, we will discuss the

reliability challenges faced when varying the device structure to enhance their operating speed. Ultimately, our aim is to develop high- performance and reliability amorphous indium gallium zinc oxide semiconductor devices that are suitable for diverse applications.

In the first section of this study, we investigate the degradation model of etch-stop-layer type amorphous-indium-gallium-zinc-oxide thin-film transistors under dynamic switching operations. We observe a severe degradation of the threshold voltage in devices after alternating current operations, while the devices exhibit high stability under direct current operations. To further analyze the degradation model, we systematically discuss the stress with different switching waveform, geometry of devices, and temperatures. The results indicate that during the transition from accumulation to depletion, electrons will perform trapping behaviors at the rear interface of the active layer. This is due to the insufficient time for the channel layer to deplete carriers under a short falling time. Then, these residual carriers in the channel are further trapped at the rear interface of the channel when switching to the off-state voltage.

In the second section of this study, we investigate the instability of amorphous-indium-gallium-zinc-oxide thin-film transistors with copper electrodes under positive gate bias stress. To elevate the operating frequency of displays, copper metal is often chosen over aluminum metal for lower resistance-capacitance delay in the metal wiring.

However, we realized that the devices will experience severe copper ion migration at the oxide layer after positive gate bias stress. We analyze the gate leakage throughout the stress duration by the carrier transport behavior in insulators to understand the degradation model. Additionally, to further observe the copper ions within the insulator layer, we used the focus ion beam system to prepare the cross-section of devices, followed by material analysis through the transmission electron microscopy system. The copper signals obtained from the material analysis directly confirm the diffusion behavior.

In the third section of this study, we integrated heterojunction channels into top-gate amorphous-indium-gallium-zinc-oxide thin-film transistors and achieved a high-performance/high-reliability transistor. The heterojunction channel is composed of two layers of indium-gallium-zinc oxide thin films with different metal ratios. The introduction of a zinc-rich layer as the front channel layer not only serves as a diffusion barrier layer which effectively suppresses the hydrogen diffusion behavior in short channel devices, but also reduces the vertical electric field in the gate insulator. To further validate this phenomenon, Silvaco TCAD simulations are conducted to systematically discuss the device characteristic and reliability of heterojunction channel thin-film transistors.

In the fourth section of this study, we demonstrate a nonvolatile optoelectronic memory through utilizing a heterojunction channel in amorphous-indium-gallium-zinc-

oxide thin-film transistors. By exploiting the carrier confinement effect of heterojunction interfaces, we separated the carrier conduction and the charge storage at the front and back bulk layers of the active region, respectively. This device exhibits a memory window of 4.6 V, a read window of 10^6, and an operating voltage requirement below 20 V. In terms of charge storage capability, the memory retains its state for over 10 years and endures more than 1000 cycles of repeated operations.

Keywords: Thin-Film Transistors, Alternating Current, Copper Diffusion, Heterojunction Channel, Nonvolatile Memory, Amorphous Indium-Gallium-Zinc Oxide

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Figure Captions

Table Captions

List of Acronyms

a-InGaZnO	Amorphous Indium-Gallium Zinc Oxide
AOS	Amorphous Oxide Semiconductor
a-Si	Amorphous Silicon
Poly-Si	Polycrystalline Silicon
FPD	Flat Panel Display
TFT	Thin-Film Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
G	Gate
S	Source
D	Drain
LCD	Liquid Crystal Display
OLED	Organic Light Emitting Diode
C_s	Storage Capacitor
AM	Active Matrix
PM	Passive Matrix
BEOL	Back-End-of-Line
M3D	Monolithic Three Dimensional
SNR	Signal-to-Noise Ratio
DRAM	Dynamic Random-Access Memory
RRAM	Resistive Random-Access Memory
I_D - V_G	Transfer Characteristic Curve
$I_D - V_D$	Output Characteristic Curve
AR	Augmented Reality
VR	Virtual Reality
ESL	Etch-Stop Layer
BCE	Back Channel Etching
PV	Passivation

GI	Gate Insulator
ILD	Inter-Layer Dielectric
DUT	Device under Test
SPGU	Semiconductor Pulse Generator Unit
PECVD	Plasma Enhanced Chemical Vapor Deposition
CVD	Chemical Vapor Deposition
FIB	Focus Ion Beam
SiOx	Silicon Oxide
SiNx	Silicon Nitride
In_2O_3	Indium Oxide
Ga_2O_3	Gallium Oxide
ZnO	Zinc Oxide
Cu	Copper
TEM	Transmission Electron Microscopy
EDS	Energy Dispersive Spectroscopy
AC	Alternating Current
DC	Direct Current
PBS	Positive Bias Stress
NBS	Negative Bias Stress
C-V	Capacitance – Voltage Characteristic Curve
BG	Bottom Gate
TG	Top Gate
FG	Floating Gate
SA	Self-Aligned
NVM	Nonvolatile Memory
TDDB	Time-Dependent Dielectric Breakdown
FBE	Floating Body Effect
F-N	Fowler–Nordheim
UV	Ultraviolet

SBH	Schottky Barrier Height
BTBT	Band-to-Band Tunneling
TAT	Trap Assist Tunneling

List of Mathematical Symbols

V_T	Threshold Voltage	V
V_{DS} (V_D)	Drain-Source Voltage	V
V_{GS} (V_G)	Gate-Source Voltage	V
V_{GD}	Gate-Drain Voltage	V
$S.S$	Subthreshold Swing	mV/dec
μ_n	Electron Mobility	cm^2/Vs
N_A	Acceptor Impurity Concentration	cm^{-3}
N_D	Donor Impurity Concentration	cm^{-3}
N_c	Conduction Band Density of State	cm^{-3}
N_v	Valence Band Density of State	cm^{-3}
ε	Vacuum Permittivity Value	8.854×10^{-12} F/m
ε_s	Semiconductor Relativity Permittivity	
ϕ_{ms}	Gate-to-Semiconductor Work Function	eV
ψ_g	Gate Work Function	eV
ψ_s	Semiconductor Work Function	eV
C_{OX}	Gate Oxide Capacitance	F/cm^2
C_{GS}	Gate to Source Capacitance	F/cm^2
Q_{OX}	Gate Oxide Charge	cm^{-2}
W	Channel Width	µm
L	Channel Length	µm
E_a	Activation Energy	eV
E_c	Conduction Band	eV
E_V	Valence Band	eV
E_g	Band Gap	eV
C_{BO}	Conduction Band Offset	eV
C_{BO}	Valence Band Offset	eV
q	Elementary Electronic Charge	1.6×10^{-19} C
t	Time	s

τ	Time Constant	
T	Temperature	K
k	Boltzmann Constant	1.38×10^{-23} m^2kg/s^2K
D_{it}	Interface Trap Density	$cm^{-2}eV^{-1}$
I_{ON}	On-State Current	A
I_{OFF}	Off-State Current	A
I_G	Gate Current	A
I_D	Drain Current	A
I_S	Source Current	A