



國立中山大學物理學系

博士論文

Department of Physics

National Sun Yat-sen University

Doctoral Dissertation

氮化鎵高電子遷移率電晶體與鰭式場效電晶體

電性及可靠度機制研究

Research on Electrical Characteristics and Reliability Mechanism of

GaN High Electron Mobility Transistors and Fin-Field Effect

Transistors

研究生：張凱鈞

Kai-Chun Chang

指導教授：張鼎張 博士

Dr. Ting-Chang Chang

中華民國 113 年 1 月

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論文審定書

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Research on Electrical Characteristics and Reliability Mechanism of GaN High
Electron Mobility Transistors and Fin-Field Effect Transistors

於中華民國 112 年 12 月 30 日經本委員會審查並舉行口試，符合博士學位論文標準。

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致謝

時光冉冉，在這充滿挑戰與成長博士班時光，不知不覺間已經是六年多的歲月。首先，我由衷地想表達對我的指導教授張鼎張老師的感謝之情。您的悉心指導與無私奉獻，使我得以在博士班的學習旅程中獲益匪淺。在學術上，您不僅提供了完善的設備和豐富的資源，給予我十分優良的學習及研究環境。除此之外，您的卓越專業和豐富經驗為我提供了寶貴的指導。尤其是您生活化的教學風格讓我受益匪淺，激發了我對學術的熱情。除了學術上的指導外，您的言教與身教更是讓我學習到面對挑戰時的正確態度。在您的引領下，我學到了如何面對困難、培養堅持不懈的毅力。是從您身上學習到的種種讓我能夠真正的翻轉出彩色人生。也非常感謝口試委員郭德明主管、蔡宗鳴老師、陳紀文執行長以及陳柏勳老師撥冗審閱我的博士論文，並提出許多寶貴的建議及獨到的見解。

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摘要

近年來，在各行業數位化和智慧型手機廣泛使用的推動下，對更高數據頻寬的需求不斷增加，推動了 5G 通訊的快速發展。此外，環保意識的增強以及電動車需求的增加，導致市場對功率元件的需求不斷增長。市場需求的這些變化引起了人們對氮化鎵 (GaN) 的極大關注。由於 GaN 具有高電子遷移率、高熱穩定性以及高崩潰電壓的優點。GaN 高電子遷移率電晶體 (HEMTs) 在高頻和高壓應用中備受期待。然而，功率轉換系統的運作總是會產生熱量。這會影響設備的其他部分，例如中央處理單元。而矽基鰭式場效電晶體 (FinFETs) 做為最廣泛應用於邏輯運算的元件，其可靠度劣化機制與環境溫度密切相關。因此，本論文主要從電學特性、可靠度測試和計算模擬方面來分析 GaN HEMTs 和矽基 FinFETs 的電性及可靠度問題。

於章節 3 中，本論文探討了 p-GaN HEMTs 的三階段關態漏電機制。藉由各端點漏電流貢獻、關態漏電重複量測實驗、低/高電壓關態應力測試及變溫關態應力測試以釐清各階段漏電機制。第一段到第三段分別由擊穿漏電、閘極電子注入以及缺陷輔助熱場發射等機制所主導。在釐清漏電機制之後，引入 un-doped GaN (UGaN) 厚度及製程溫度等變因並且為調整漏電特性的製程改進提供了可行的途徑。實驗結果顯示薄 UGaN 以及較低的製程溫度對於擊穿漏電的抑制效果最好。此外，厚 UGaN 能夠較好地抑制第三階段的產生電流。

於章節 4 中，本論文探討了在 p-GaN HEMTs 中低/高碳摻雜濃度緩衝層之間

的異常飽和區電流趨勢。在飽和區下具有高碳摻雜濃度緩衝層的 p-GaN HEMTs 具有較高的電流。這一結果與碳摻雜會降低 2DEG 濃度的通常認知相違背。藉由變溫實驗以及飽和區應力測試釐清此異常趨勢背後的原因。這是由於低碳摻雜濃度緩衝層的 p-GaN HEMTs 中 GaN 層的能障較低。在飽和區條件下較容易於 GaN 層中發生熱電子注入進而影響電流特性。最後，碳摻雜濃度對能障的影響透過 Silvaco TCAD 模擬進行了驗證。

於章節 5 中，本論文探討了肖特基閘極 GaN HEMTs 的 Drain-induced barrier lowering (DIBL) 效應飽和現象。透過 Silvaco TCAD 模擬不同 V_d 的電場、能帶以及 2DEG 濃度，並藉此分析出 DIBL 效應飽和現象是源自於 T 型閘極結構。T 型閘極結構具有在大 V_d 下空乏額外的 2DEG 的能力。因此能夠在大 V_d 下分散本應集中於通道的電場，進而抑制 DIBL 效應。最後，從寄生電容的角度探討了抑制 DIBL 的能力與 T 型閘極的幾何間的關係。

於章節 6 中，本論文探討了 60nm 和 14nm FinFET 中溫度對於熱載子劣化機制的影響。藉由機制的擬合釐清不同電壓條件下的劣化機制。隨著 V_g 的增加，HCS 劣化機制從電場相關性相對較高的 Single Vibrational Excitation (SVE) 或 Electron-Electron Scattering (EES) 轉變為電場相關性較低的 Multiple Vibrational Excitation (MVE) 機制。在 60nm 樣品中，由於聲子散射的影響，隨著溫度的升高，以 SVE 為主的部分轉變為 EES 機制。由於溫度對於電子間散射的增幅。高溫下的 14nm 樣品，在更高的 V_g 從 EES 轉變為 MVE。最後，lifetime (τ) 和溫度

之間的關係驗證了這個論點。

關鍵字：氮化鎵高電子遷移率電晶體、關態漏電、汲極引發位能障降低、鰭式場效電晶體、熱電子效應

Abstract

In recent years, the growing demand for higher data bandwidth, driven by digitalization across various industries and the widespread use of smartphones, has fueled the rapid development of 5G communication. Additionally, the increasing awareness of environmental concerns and the rising demand for electric vehicles have led to a continuous growth in the market's demand for power devices. These shifts in market demand have prompted significant attention toward Gallium Nitride (GaN). GaN is highly regarded for its advantages, including high electron mobility, excellent thermal stability, and a high breakdown voltage. Therefore, GaN High Electron Mobility Transistors (HEMTs) are particularly anticipated for high-frequency and high-voltage applications. However, power conversion systems always generate heat during operation, which can affect other components, such as central processing units. Silicon-based Fin Field-Effect Transistors (FinFETs), as the most widely used devices in logic operations, exhibit degradation mechanisms closely related to environmental temperature. Therefore, this dissertation primarily focuses on analyzing the electrical characteristics and reliability issues of GaN HEMTs and silicon-based FinFETs through electrical properties, reliability testing, and electrical simulations.

In Chapter 3, this dissertation explores the three-stage leakage mechanisms in p-GaN HEMTs. Through the investigation of leakage current contributions at various

endpoints, repeated experiments on leakage measurements, low/high voltage off-state stress tests, and temperature-dependent off-state stress tests, the mechanisms at each stage are clarified. These stages are primarily dominated by punch-through leakage, gate electron injection, and defect-assisted thermal field emission. Once the leakage mechanisms are elucidated, the introduction of variables like un-doped GaN (UGaN) thickness and process temperature provides a feasible pathway for adjusting leakage characteristics through process improvements. Experimental results ultimately reveal that a thin UGaN layer and lower process temperatures offer the more effective suppression of punch-through leakage. Conversely, a thick UGaN layer is more effective in curbing current generation.

In Chapter 4, the dissertation examines the anomalous saturation current trends between p-GaN HEMTs with low and high carbon doping concentration buffer layers. The p-GaN HEMTs with high carbon doping concentration buffer layers exhibit higher current levels in the saturation region. This result contradicts the common understanding that carbon doping reduces 2DEG concentration. The reasons behind this anomalous trend are clarified through temperature experiments and saturation region stress tests. This anomaly is due to the lower energy barrier in the GaN layer of p-GaN HEMTs with low carbon doping concentration buffer layers. Under saturation region conditions, hot electron injection into the GaN layer occurs more easily, affecting current characteristics.

Lastly, the impact of carbon doping concentration on the energy barrier is verified through Silvaco TCAD simulations.

In Chapter 5, this dissertation investigates the Drain-Induced barrier lowering (DIBL) effect saturation phenomenon in Schottky-gate GaN HEMTs. Utilizing Silvaco TCAD simulations involving electric fields, energy band diagrams, and 2DEG concentrations at various drain voltage (V_d), the analysis reveals that the saturation of the DIBL effect is rooted in the T-gate structure. This gate structure has the ability to deplete additional 2DEG under large V_d , thus dispersing the electric field that would normally concentrate in the channel, consequently suppressing the DIBL effect. Finally, the thesis examines the relationship between the ability to suppress DIBL and the geometric aspect of the T-gate structure from the perspective of parasitic capacitance.

In Chapter 6, this dissertation explores the influence of temperature on the degradation mechanisms in 60nm and 14nm FinFETs. Through fitting the mechanisms, the impact of different voltage conditions on degradation mechanisms is clarified. With increasing gate voltage (V_g), the Hot Carrier Stress (HCS) degradation mechanism transitions from Single Vibrational Excitation (SVE) or Electron-Electron Scattering (EES) mechanisms with relatively higher field dependence to the Multiple Vibrational Excitation (MVE) mechanism with lower field dependence. In the 60nm sample, due to the impact of phonon scattering, the part predominantly governed by SVE transitions to

the EES mechanism as the temperature rises. In the 14nm sample at higher temperatures, under higher V_g , the transition shifts from EES to MVE. Finally, the relationship between lifetime (τ) and temperature validates this argument.

Keywords: GaN HEMTs, Off-state Leakage, Drain Induced Barrier Lowering, FinFETs, Hot Electron Effect

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