國立中山大學物理學系

博士論文

Department of Physics

National Sun Yat-sen University

Doctoral Dissertation

次世代高功率元件之電性分析與可靠度探討

Investigation on Electrical Analysis and Reliability Issues in Next-Generation High-Power Devices

研究生：洪瑋駿

Wei-Chun Hung

指導教授：張鼎張 博士

Dr. Ting-Chang Chang

中華民國 113 年 1 月

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Investigation on Electrical Analysis and Reliability Issues in Next-Generation High-Power Devices

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摘要

近年來，隨著電動車及汽車智慧化的浪潮興起，車用晶片的需求也逐漸在增加，並且在汽車總成本佔據的成本比例也逐年提升，從 1950 年的 1%成長至 2030 年的 50%。其中又以電源管理晶片(PMIC)扮演重要角色，其能夠實現 DC 電源保護、低靜態漏電和降低電磁干擾等特性，可以有效提升電動車的續航力以及傳統汽車的燃油效率。應用場景包括先進駕駛輔助系統(ADAS)、數位座艙(digital Cockpit)、電池管理等。因此 PMIC 相關元件的性能與可靠度可謂非常重要的一環。

先進的 PMIC 主要採用 Bipolar-CMOS-DMOS (BCD)技術，在單一晶片上整合三種不同類型的元件，並提取各自的優點與功能，包括：(1) Bipolar 具高操作電流、高線性轉導和低 1/f 雜訊等特性，用於放大訊號；(2) CMOS 具小尺寸、抗干擾和節能，用於數位運算；(3) DMOS 的高電壓耐受性，用於高功率驅動。在 BCD 技術中，理想的 DMOS 具有低開態電阻和高崩潰電壓特性。在降低開態電阻部分，DMOS 採用接觸場板結構(Contact Field Plate, CFP)，將場板與閘極連接，覆蓋部份漂移區域，吸引漂移區的少數載子，可以降低漂移區的電阻，使整體開態電阻下降。在提高崩潰電壓部分，透過高耐壓低表面電場設計，提高漂移區的耐壓程度。由於 CFP 的出現，LDMOS 的整體性能提高了，但在可靠度方面卻仍存在嚴重的問題。

本論文第一部分研究為 LDMOS 在未導通應力的可靠度測試。由於 LDMOS 是開關元件，所以會常時間操作在關態的狀況下，此時高電壓會施加在汲極端，可能導致元件的劣化發生，故如何提升 LDMOS 在未導通應力下的可靠度是一重要議題。研究中發現 LDMOS 元件在經過一段時間的未導通應力測試後，會產生嚴重的開態電流下降問題。分析其原因係在元件的阻障保護氧化層(Resist Protective Oxide, RPO)中，在導通應力過程中，因電場影響使電子注入到 RPO 中，導致元件飄移區的電阻上升，最終使開態電阻受到影響，進而增加元件的功率消耗。因此，若能有效改善 CFP 層品質則能大幅提升 LDMOS 的應用價值。

本論文第二部分研究為 LDMOS 在熱載子不穩定性測試下的可靠度問題，在開關元件進行切換時，會經過高電壓高電流的操作區域，這時會使元件中的載子得到巨大的能量，進而產生大量的熱載子，使元件在介面處受到劣化。在研究中 LDMOS 元件在經過一段時間的 HCI 後，發現到開態電流下降與臨界電壓(threshold voltage, V_{th})偏移問題。針對這個現象，分析其劣化機制分為兩個階段。第一階段是在接觸場板結構下發生碰撞游離導致電子注入 RPO，導致開態電流劣化。第二階段劣化是焦耳熱引起的正偏壓溫度不穩定性效應(Positive Bias Temperature Instability, PBTI)，導致元件中 SiO_2/Si 介面出現缺陷，並將通道中的電子注入到 SiO_2 中，從而增加了元件的次臨界擺幅，並導致 V_{th} 發生變化。 通過溫度變化實驗和 TCAD 模擬證明，在長時間的熱載子不穩定性測試過程中，熱載子不穩定性測試確實會產生嚴重的 PBTI 並導致元件劣化。LDMOS 的性能與可靠度需要進一步釐清，分析其物理機制，提升整體特性，確保在 PMIC 中可安全的運行。

本論文第三部分為研究藉由超臨界流體技術，提升快速回復二極體(Fast Recovery Diodes, FRD)的性能。一般而言，MOSFET 在製作會因為元件本身結構，生成內建的體二極體。此二極體可以保護 MOSFET 在施加反向電壓時不會崩潰。但在開關電源中，因為需要高速的切換，所以二極體的動態特性對 MOSFET 整體性能影響很大。若要提升元件效率一般會額外並聯 FRD 元件，提升開關效率。為了達到快速切換的條件，FRD 會參雜金屬作為二極體的複合中心，藉此增加少數載子複合的速度，以提升切換速度。但在摻雜金屬的同時會增加 Si 中的能階，導致元件漏電流增加。此章節將藉由超臨界流體技術鈍化掉元件中的缺陷，使 FRD 在不影響切換特性的情況下降低漏電流。並且也同時透過電容-電壓特性曲線發現缺陷產生的位置，並進一步提出對應的物理模型。

關鍵字:功率半導體元件、雙極-互補金屬氧化半導體-雙重擴散金屬氧化半導體、橫向擴散金屬氧化物半導體、非導通應力測試、熱載子應力測試、快速回復二極體、超臨界流體

Abstract

In recent years, the demand for automotive chips has been increasing with the rise of electric vehicles and intelligent vehicles. The cost of automotive chips in the overall vehicle cost has also been increasing year by year, from 1% in 1950 to 50% in 2030. Among them, power management ICs (PMICs) play an important role in automotive electronics. They can realize DC power protection, low static leakage current, and reduce electromagnetic interference, which can effectively improve the battery life of electric vehicles and the fuel efficiency of traditional vehicles. Applications cover advanced driver assistance systems (ADAS), digital cockpits, and battery management. Therefore, the performance and reliability of PMIC-related components are very important.

Advanced PMICs mainly use bipolar-CMOS-DMOS (BCD) technology to integrate three different types of components on a single chip, and extract their own advantages and functions, including: (1) Bipolar has high operating current, high linear transfer, and low 1/f noise characteristics, which are used for signal amplification; (2) CMOS has small size, anti-interference, and energy saving, which are used for digital computing; (3) The high voltage tolerance of DMOS is used for high-power driving. In BCD technology, the ideal DMOS has low on-state resistance (R_{on}) and high breakdown voltage (V_{bd}). To reduce R_{on}, DMOS uses a contact field plate (CFP) structure, which connects the field plate to the gate, covers part of the drift region, and attracts minority carriers in the drift region, which can reduce the resistance of the drift region and lower the overall R_{on}. To improve V_{bd}, the reduced-surface-field (RESURF) is used to improve the withstand voltage of the drift region. The emergence of the CFP structure has improved the overall performance of LDMOS, but there are still serious problems in terms of reliability.

This work studies the reliability of LDMOS under non-conducting stress (NCS) and hot carrier instability (HCI) tests. In the NCS test, it is found that LDMOS devices will have a serious problem of linear region on-state current (I_{on}) decrease after a period of time. The analysis shows that the reason is in the resist protective oxide layer (RPO) of the device. In the NCS process, the electrons are injected into RPO due to the influence of the electric field, which causes the resistance of the drift region of the device to rise, and finally affects R_{on}, which in turn increases the power consumption of the device. Therefore, if the quality of RPO can be effectively improved, it can greatly improve the application value of LDMOS.

In the HCI test, it is found that LDMOS devices will have I_{on} decrease and threshold voltage (V_{th}) shift problems after a period of time. The analysis shows that the degradation mechanism can be divided into two stages. The first stage is the collision ionization that occurs under CFP, which leads to electron injection into RPO, resulting in I_{on} degradation. The second stage of degradation is the positive bias temperature instability (PBTI) effect caused by Joule heat, which causes defects at the SiO_2/Si interface in the device, and injects the electrons from the channel into SiO_2, thereby increasing the subthreshold swing (S.S.) of the device and causing V_{th} to change. Through temperature variation experiments and TCAD simulation, it is proved that HCI will indeed produce serious PBTI effects and cause device degradation in the long-term HCI process.

In the third part of this work, we study the performance improvement of fast recovery diodes (FRD) by using supercritical fluid technology. Generally, MOSFETs will generate an internal body diode due to their own structural characteristics during the manufacturing process. This diode can protect MOSFETs from collapsing when an inverse voltage is applied. However, in switch power applications, because the diodes need to be switched quickly, the dynamic characteristics of the diodes have a great impact on the overall

performance of MOSFETs. In order to improve the efficiency of the device, FRD are usually connected in parallel to improve the switching efficiency. In order to achieve the condition of fast switching, FRD are doped with metal as the recombination center of the diode, so as to increase the recombination speed of minority carriers, so as to improve the switching speed. However, the addition of metal will increase the energy level in Si, which will lead to an increase in leakage current. In this section, using supercritical fluid technology to passivate the defects in the devices, so that FRD can reduce leakage current without affecting the switching characteristics. It will also use the capacitance-voltage (C-V) characteristic curve to find the location of the defects and further propose the corresponding physical model.

Keywords: Power Semiconductor devices, Bipolar-CMOS-DMOS (BCD), LDMOS, Non-conducting stress (NCS), Hot carrier injection (HCI), Fast recovery diodes (FRD), Supercritical fluid.

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