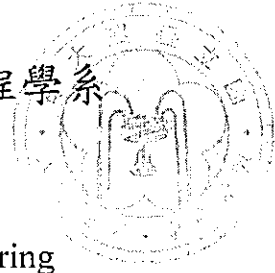


國立臺灣大學工學院材料科學與工程學系



博士論文

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Doctoral Dissertation

探索無外加磁場自旋軌道矩機制以實現高效能磁性與
類神經形態記憶體系統

Exploring Field-Free Spin-Orbit Torque Mechanisms for
High-Efficiency Magnetic and Neuromorphic Memory
Systems

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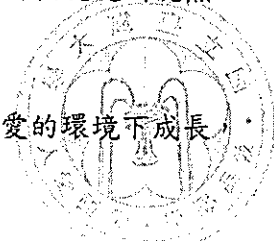
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摘要

在人工智慧(AI)時代，次世代記憶體技術受到高度關注，需具備節能、高密度以及可類比編程等特性，以支援大規模神經形態運算。自旋軌道矩(SOT)裝置因其具有非揮發性、高耐久性與互補式金屬氧化物半導體(CMOS)製程相容性而備受關注，更重要的是，它能透過磁區壁運動等穩定且可控制的物理機制，實現可靠的類比切換行為。此一穩定性優於其他次世代記憶體技術，如電阻式記憶體(RRAM)與相變記憶體(PCM)，使自旋軌道矩裝置特別適合用於多位元突觸權重的實現。

本論文研究三種不需外加磁場的自旋軌道矩切換機制：包括尼爾橘皮效應、膜層間 Dzyaloshinskii-Moriya 交互作用以及傾斜磁異向性。這些機制皆透過微米尺寸的霍爾量測元件進行實驗，並以鎢(W)與鉑(Pt)為基底材料進行異質結構製作。為系統化比較各裝置表現，本研究建立統一的評估架構，涵蓋切換效率、熱穩定性、可分辨的電阻狀態數與週期間變異性等關鍵指標。

在所有測試裝置中，傾斜磁異向性樣品展現最佳的類比行為，能穩定實現 11 個量化的電阻狀態，且週期間變異性低於 3%，有助於實現穩定的多位元權重表示。進一步引入銥錳反鐵磁層(IrMn)可提升熱穩定性，但會降低類比切換能力。為了與類比設計進行比較與互補，本研究亦展示一種數位型自旋突觸，透過將四個二進位的自旋軌道轉矩記憶體元件組合成一個突觸，實現 2 位元權重解析度與更高的操作穩定性。

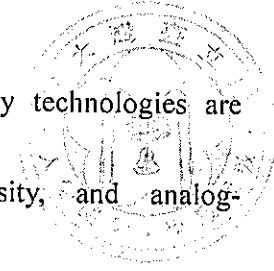
本研究進一步將微米尺寸霍爾元件的量測特性投射至實際的自旋軌道轉矩記憶體(SOT-MRAM)架構中，以進行系統層級的效能評估。使用 NeuroSim 模擬平台，在 32 奈米製程節點下，針對類比型與數位型自旋軌道轉矩記憶體，以及傳統靜態隨機存取記憶體(SRAM)進行電路層級模擬與比較。結果顯示，數位型設計於 MNIST 手寫辨識資料集上可達 92.2% 的推論準確率，且讀取能耗與延遲皆低於靜態隨機存取記憶體；類比型設計則展現出更優異的能源效率，但為達成相似的推論準確率，仍需克服隧道磁阻比不足的挑戰。

本論文建立一套完整的無外場自旋軌道矩裝置之實驗與建模分析框架，並針對材料設計、裝置架構與電路整合提出關鍵見解，希冀有助於未來自旋記憶體與神經形態運算系統的發展與應用。



關鍵詞：自旋電子學、零外場自旋軌道轉矩切換、類比自旋電子突觸、神經形態運算。

ABSTRACT



In the era of artificial intelligence (AI), emerging memory technologies are increasingly expected to provide energy-efficient, high-density, and analog-programmable capabilities to support large-scale neuromorphic computing. Spin-orbit torque (SOT) devices stand out not only for their non-volatility, high endurance, and complementary metal-oxide-semiconductor (CMOS) compatibility, but more importantly, for their ability to robustly realize analog switching behaviors through physical mechanisms such as domain wall propagation. This level of stability exceeds that of other emerging memories such as resistive random access memory (RRAM) and phase change memory (PCM), making SOT devices particularly suitable for implementing multi-level synaptic weights in neuromorphic architectures.

This dissertation investigates three field-free current-induced SOT switching mechanisms: the Néel orange-peel effect, interlayer Dzyaloshinskii-Moriya interaction (i-DMI), and tilted magnetic anisotropy. These mechanisms are experimentally studied using micron-scale Hall bar devices fabricated from W- and Pt-based heterostructures. A unified benchmarking framework is developed to quantify switching efficiency, thermal stability, analog programmability, and cycle-to-cycle (CTC) variation.

Among the evaluated devices, the tilted anisotropy sample demonstrates the best analog behavior, achieving 11 clearly separated resistance states with less than 3% CTC variation. This supports stable multi-level weight representation for neuromorphic

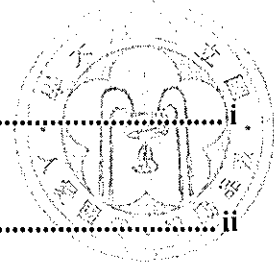
computing. The introduction of an IrMn antiferromagnetic layer further improves thermal stability but limits analog switching. A digital spintronic synapse is also demonstrated by grouping four binary SOT device cells to achieve 2-bit resolution and enhanced robustness to complement analog designs.

The measured characteristics from micron-scale Hall bar devices are projected onto practical SOT- magnetic random access memory (MRAM) architectures to enable system-level evaluation. Subsequently, device-to-circuit simulations are performed using NeuroSim at the 32 nm technology node to benchmark analog SOT-MRAM, digital SOT-MRAM, and SRAM. Digital SOT-MRAM achieves 92.2% inference accuracy on the MNIST dataset, with lower read energy and latency than SRAM. The analog design shows comparable energy-delay benefits but requires a higher ON/OFF ratio to reach similar accuracy.

This work establishes a comprehensive experimental and modeling framework for field-free SOT devices and provides insights into material engineering, device architecture, and circuit-level integration for future spintronic memory and neuromorphic systems.

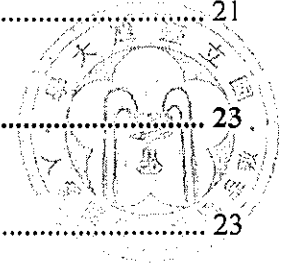
Keywords: Spintronics, field-free spin-orbit torque (SOT) switching, analog spintronic synapse, neuromorphic computing.

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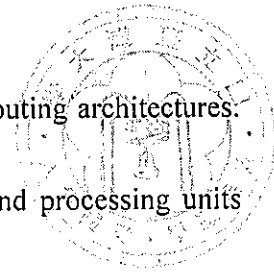


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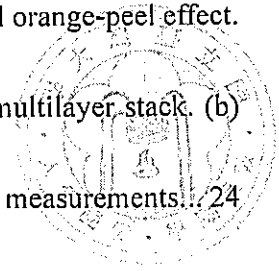


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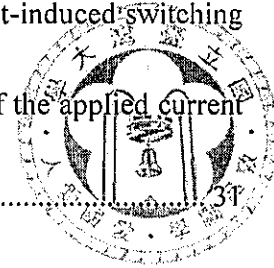


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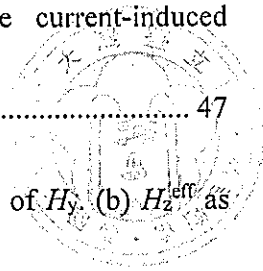


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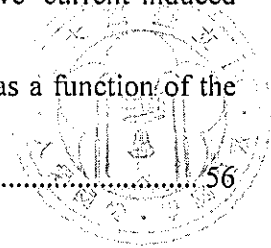


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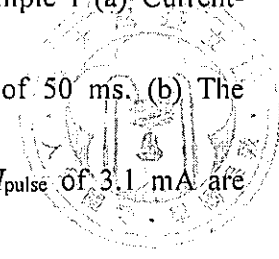


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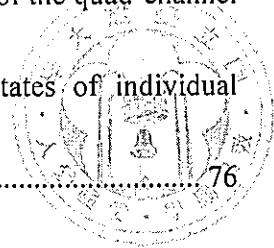


Fig. 6.3 System-level evaluation of digital and analog SOT synapse implementations. (a)

Circuit schematic of a single-cell analog SOT-MRAM device with a 2T1R configuration. (b) Circuit schematic of a digital SOT-MRAM synapse composed of four binary cells ($N = 4$) to represent 2-bit weights. (c) Schematic of the two-layer MLP neural network architecture used for NeuroSim simulations, consisting of 400 input neurons, 100 hidden neurons, and 10 output neurons for MNIST digit recognition. (d) Inference accuracy as a function of the conductance ON/OFF ratio..... 79

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